

Orthogonal photopatterning of two-dimensional percolated network films for wafer-scale heterostructures

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Molecular intercalation-based electrochemical exfoliation of two-dimensional (2D) materials can be used to create van der Waals heterostructures. However, the scalable assembly of vertical heterostructures typically requires the use of various chemical solvents for photolithography and subsequent transfer, which can leave behind chemical residues and limit the patterning resolution. We show that patterned van der Waals heterostructures can be fabricated from electrochemically exfoliated 2D flakes using a photoreactive crosslinker. When a 2D van der Waals percolated network with the crosslinker is exposed to ultraviolet light, the network junctions form covalent bonds, thereby enabling improved charge transport and orthogonal patterning of vertically stacked van der Waals thin-film networks without affecting the underlying prepatterned layers. Our approach can be used to create wafer-scale arrays of photopatterned field-effect transistors based on different 2D materials. The field-effect transistors exhibit high spatial uniformity and can be used to create logic gates, namely NOT, NAND and NOR gates.

Solution-processed two-dimensional (2D) materials are a promising material platform for next-generation thin-film electronics^{1–3}. In pursuit of such materials, molecular intercalation-based electrochemical exfoliation could potentially overcome the limitations of conventional solution-based exfoliation methods^{4,5}, such as liquid-phase exfoliation, which produces nanoflakes with small lateral dimensions (often less than 100 nm) and non-uniform thicknesses due to the high mechanical energy applied, resulting in a porous thin-film network with high flake-to-flake contact resistance⁶. In molecular intercalation-based electrochemical exfoliation, in which the intercalation of bulky organic

molecules into layered crystals expands their interlayer distance and weakens the van der Waals bonds, fully exfoliated 2D flakes can be produced with minimal applied mechanical energy (such as mild sonication), enabling the scalable production of atomically thin 2D nanosheets^{7–10}. The resulting samples can exhibit large lateral dimensions (often more than 1 μm), high aspect ratios and atomically clean surfaces, so that they can be assembled into electronically active mosaic-like thin films at wafer scale.

When assembled into thin films, these consist of conformal van der Waals plane-to-plane contacts over large overlapping areas^{10,11}.

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Because of the van der Waals interaction between nanosheets, efficient charge transport through nanosheet-to-nanosheet junctions has been achieved and used to create electronic devices, including field-effect transistors (FETs)^{12,13}, photodetectors^{14,15} and logic gates¹⁶. Notably, these van der Waals thin films enable the development of high-performance electronics (average carrier mobility around $10\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, in general) at the array level, with electronic performance approaching that of 2D materials grown by chemical vapour deposition¹⁷. Furthermore, by leveraging the versatility of the exfoliation strategy, electronically distinct thin films with metallic, semiconducting or insulating properties, can be created on a large scale¹⁸.

Efficient charge transport through intersheet junctions based on the van der Waals interaction has also been examined by forming van der Waals heterostructures through vertical stacking of heterogeneous 2D nanosheets^{19,20}. This allows the intrinsic physical properties to be maximized. Owing to their ultrafast charge transfer and strong inter-layer coupling, exotic phenomena can be created, such as Mott-like insulators, topological superconductivity and moiré excitons^{21–24}. Typically, such vertical heterostructure-based devices are fabricated using individual 2D nanosheets that have been micromechanically exfoliated and transferred in a microscopy-assisted manner to ensure precise positioning and angles with respect to the pre-positioned 2D layers^{20,25,26}. However, the complexity of this process confines its use to prototype devices. To create vertical van der Waals heterostructures on a large scale, 2D materials must be laterally assembled into a thin film before being vertically integrated with other thin films with different electronic properties^{27,28}. Although 2D materials can be integrated into mosaic-like thin-film structures or sandwich-like van der Waals heterostructures by lateral and vertical assembly, respectively, the lack of an appropriate patterning process makes it challenging to achieve both at wafer scales^{29–32}.

To exploit mosaic-like thin films in scalable van der Waals heterostructures, two key requirements must be satisfied. First, a patterning process must be used that leaves minimal chemical residues and defects on the surface. Second, it must use an integration process that does not have any detrimental effect on each layer. The method most commonly used to pattern 2D material thin films is photolithography³³. However, conventional lithography processes can introduce chemical residues from substances such as photoresist and developers, which can result in undesired defect states, chemical doping and organic diffusion^{34,35}. These residues can critically hinder the creation of high-quality van der Waals interfaces, leading to increased junction resistance and charge trapping and lower device performance. To mitigate this issue, 2D material thin films have been transferred onto a prepatterned negative photoresist layer^{25,36}. However, the characteristics of a negative photoresist can compromise the minimum resolution of the resulting patterns. Furthermore, it is difficult to find solvents that do not disrupt the underlying prepatterned layer (that is, are orthogonal) or to successfully transfer the resulting films. Other approaches—such as screen printing, inkjet printing^{37,38} and adhesion energy-engineered patterning methods³⁹—suffer from low resolution, uniformity, reliability on a large scale or chemical robustness.

In this article, we describe an approach—termed photoresist-free, orthogonal multi-patterning of thin films (PROMPT)—to create solution-processed 2D materials and integrate them into scalable vertical van der Waals heterostructures. We used the strategy to create well-defined patterns (as small as $5\text{ }\mu\text{m}$) in different 2D materials, namely semiconducting molybdenum disulfide (MoS_2), insulating hafnium oxide (HfO_2) (oxidized from hafnium disulfide (HfS_2)) and conducting graphene. First, to pattern the films, a crosslinking agent with photoreactive moieties is used that induces crosslinking upon ultraviolet (UV) irradiation through a photomask. After the photo-induced crosslinking, the resulting 2D material network film exhibits superior chemical robustness against exposure to various chemical solvents compared with uncrosslinked pristine 2D material films. This allows

the electrical characteristics of the film to be preserved during the photopatterning of subsequent layers, thus enabling the orthogonal patterning of vertically stacked van der Waals films.

Additionally, because the amount of chemical residue is lower compared with conventional photopatterning processes, the 2D material network films exhibit a clean surface, which allowed us to fabricate a stacked heterostructure with high-quality interfaces and, thus, negligible hysteresis and good device stability. We used our PROMPT approach to create a wafer-scale FET array based on vertically integrated 2D material network films. The devices had an average electron mobility $\mu_e = 20.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and hysteresis-free characteristics. We used the photopatterned FETs to create various logic gates, namely NOT, NAND and NOR gates.

Photopatterned 2D vertical van der Waals heterostructures

Figure 1a schematically illustrates the atomic structure of the 2D materials and the proposed PROMPT process-based van der Waals heterostructure integration. The van der Waals heterostructure comprised insulating HfO_2 (oxidized from HfS_2), semiconducting MoS_2 and metallic graphene as a dielectric layer, a channel and electrodes, respectively. The layers were prepared by molecular intercalation-based electrochemical exfoliation (Supplementary Fig. 1). The exfoliation process for the 2D materials is described in detail in Methods. Ethane-1,2-diyl bis (4-azido-2,3,5,6-tetrafluorobenzoate), which contains two photoactive phenyl azide moieties ($-\text{N}_3$) at both termini of the molecule (see the upper part of Fig. 1b), was employed as a photoresponsive crosslinker for the UV-induced crosslinking process, as shown in Fig. 1b. The phenyl azide moieties can generate a reactive singlet nitrene intermediate (^1N) upon UV light irradiation with a wavelength of 254 nm while releasing nitrogen (N_2) gas. The reactive ^1N can readily undergo a C–H insertion reaction with neighbouring alkyl chains to form crosslinked functional materials^{40,41}. Note that polyvinylpyrrolidone (PVP) was added to stabilize the 2D nanosheet in chloroform. Even after purification, a trace amount of this polymer remained as a residual surfactant in the 2D materials. The alkyl chains of the residual PVP were harnessed to accommodate the reaction sites for as-generated ^1N , and the C–H insertion reaction assisted in ensuring a photo-induced crosslinking network at the nanosheet-to-nanosheet interfaces. The covalent junctions that formed locally in the crosslinked regions increased the mechanical stability of the 2D layers, which preserved their structure even after ultrasonication in a solvent, thereby enabling orthogonal patterning. Moreover, only a small amount of crosslinker ($<5\text{ wt}\%$) was employed, and thus, the additives only marginally affected the inherent electrical characteristics of the 2D nanosheets. The abovementioned photochemical reaction of the crosslinker in the overlapping 2D nanosheets was evaluated by employing Fourier-transform infrared spectroscopy to monitor the characteristic peaks associated with the N_3 moieties ($\sim 1,215\text{ cm}^{-1}$) before and after UV light irradiation, as shown in Supplementary Fig. 2.

As shown in Fig. 1c, this photopatterning strategy is widely applicable to various 2D materials, including semiconducting MoS_2 , insulating HfO_2 and metallic graphene (upper optical microscopy images from left to right), which have periodically aligned line patterns (linewidth and gap of 6 and $4\text{ }\mu\text{m}$, respectively) with the appropriate thickness for optimized performance in potential FET applications. Atomic force microscopy (AFM) images of the patterned 2D materials are shown in Supplementary Fig. 3. Additionally, various patterns (lower images in Fig. 1c and Supplementary Fig. 4) highlight the potential applicability of our photopatterning strategy. The patterned 2D networks maintained their uniform surface morphology even when scaled up to a 6-inch wafer (Supplementary Fig. 5). This uniformity was achieved by the natural alignment of basal planes parallel to the substrate during the coating of the 2D dispersion, which arises from the structural features of 2D materials (large lateral size and uniform thickness) (Supplementary Figs. 1 and 6). Consequently, the 2D network stacks are parallel to

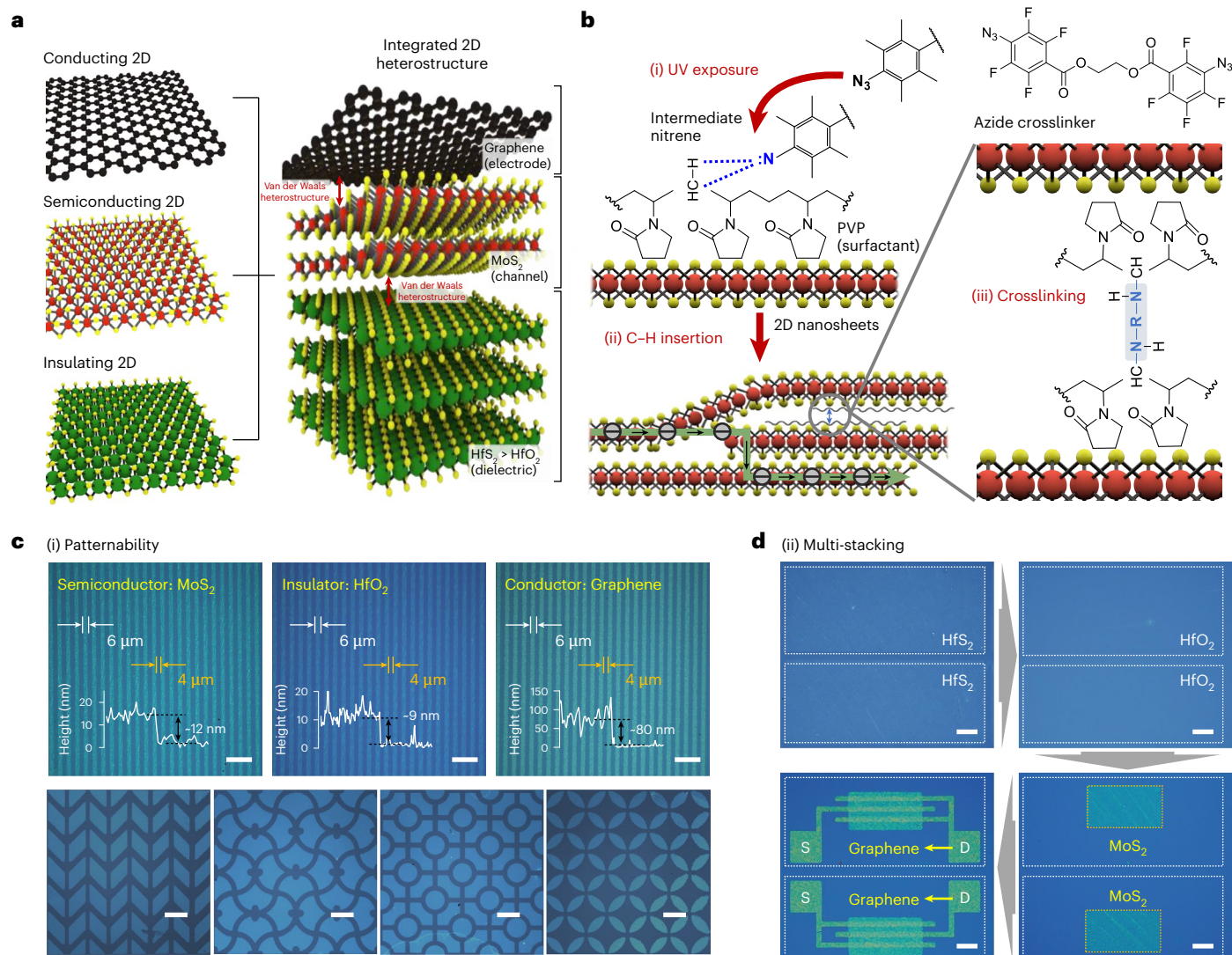


Fig. 1 | Photopatterned 2D vertical van der Waals heterostructures.

a, Schematic illustration of the 2D materials and van der Waals heterostructure assembled with metallic graphene, semiconducting MoS₂ and insulating HfO₂ (oxidized from HfS₂). **b**, Schematic description of the photo-crosslinking process between neighbouring 2D nanosheets based on the C–H insertion reaction

with PVP surfactants. **c**, Optical microscopy images of various 2D van der Waals patterns fabricated by direct photopatterning. **d**, Optical microscopy images of the fabrication procedures for the 2D material-based FETs. Scale bars, 30 μm (**c**, top row), 500 μm (**c**, bottom row), 200 μm (**d**). D, drain; S, source.

each other, resulting in low surface roughness (Supplementary Fig. 7). Owing to these characteristics, the uniform deposition of the 2D network is guaranteed when the second layer is coated on the prepatterned layer, as verified by the uniform height step and the lack of major differences in the root-mean-square (r.m.s.) roughness between the prepatterned HfO₂/MoS₂ region and MoS₂ region (Supplementary Fig. 8).

The most distinctive advantage of this crosslinker-based direct photopatterning approach over conventional photolithography is its ability to achieve multi-stacking integration without the need for orthogonal solvents that disrupt the underlying prepatterned layers. This approach was used to fabricate a typical FET structure with a bottom-gate, top-contact configuration by combining vertically stacked insulating HfO₂, semiconducting MoS₂ and metallic graphene layers as a dielectric layer, a channel, and source and drain electrodes, respectively. As shown in the optical microscopy images in Fig. 1d, the vertically stacked 2D heterostructures were sequentially assembled by repeating a unit process that encompassed the spin-coating of a dispersion of the 2D material and crosslinker mixture, UV exposure and ultrasonication for development. A mixture solution containing HfS₂ nanosheets and the crosslinker in chloroform was spin-coated

onto a heavily doped Si substrate to fabricate the FET. Thereafter, the as-deposited HfS₂ film was exposed to UV light through a photomask and then ultrasonicated in fresh chloroform to remove the uncrosslinked regions. Subsequently, the resulting photopatterned HfS₂ films were converted into insulating HfO₂ through a thermal oxidation process at 500 °C for 5 h under ambient conditions. The thermal decomposition profiles of the crosslinker and PVP obtained from a thermogravimetric analysis are shown in Supplementary Fig. 9. Similarly, each dispersion of semiconducting MoS₂ and metallic graphene with the crosslinker was consecutively processed onto the prepatterned layer(s) to form the desired structures. The photopatterning process can be successfully applied sequentially because of the chemical robustness of the underlying crosslinked layers against repeated subsequent patterning processes for the upper layers.

Chemical and electrical analyses of 2D percolated networks

As shown in Fig. 2, the electronic properties of each 2D material, namely semiconducting MoS₂, metallic graphene and oxidized HfS₂ as a dielectric, were characterized before the materials were assembled

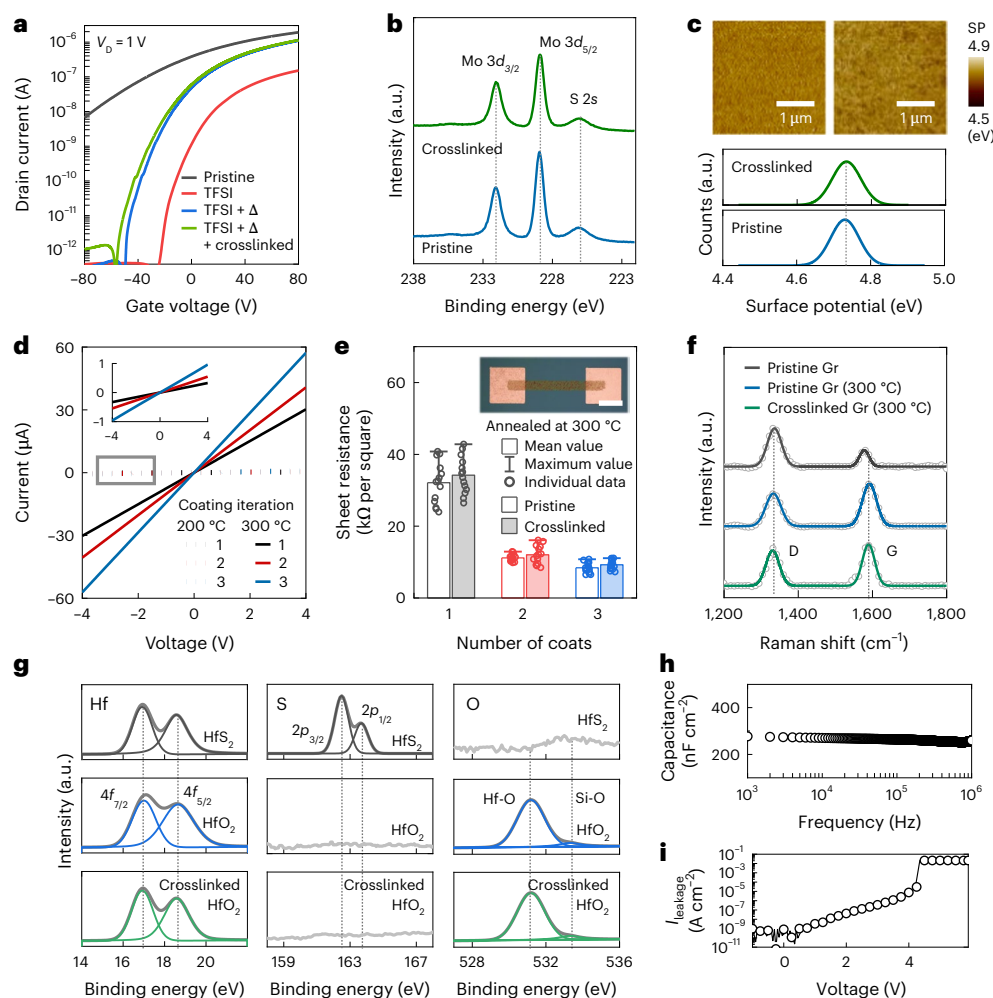


Fig. 2 | Chemical and electrical analyses of 2D percolated networks.

a, Electrical-transfer curves of the pristine MoS₂-containing (grey), TFSI-doped (red), thermally annealed (blue) and photo-crosslinked (green) FETs. **b**, XPS spectra of TFSI-doped and thermally annealed MoS₂ (blue) and crosslinked MoS₂ (green) fitted to deconvolute Mo 3d_{3/2}, Mo 3d_{5/2} and S 2s intensities. **c**, Kelvin probe force microscopy images and extracted surface potential of MoS₂ and crosslinked MoS₂ with optimized TFSI doping. **d**, Current as a function of the voltage of graphene with respect to the number of coating iterations and thermal annealing temperature. Inset, Zoom-in of crossover region. **e**, Sheet resistance of graphene and crosslinked graphene as a function of coating iteration at an

annealing temperature of 300 °C. Data are presented as mean values. The upper part of a whisker marks the maximum value ($n = 14$ measurements from distinct samples). Inset: optical microscopy image of the device consisting of Au metal electrodes (square) and a graphene conductive path (rectangle). **f**, Raman spectra of pristine graphene (grey), annealed graphene (blue) and crosslinked annealed graphene (green). **g**, XPS spectra of HfS₂ (top), HfO₂ oxidized from HfS₂ (middle) and crosslinked HfO₂ (bottom). **h**, Specific capacitance as a function of the frequency of crosslinked HfO₂. **i**, Leakage current with respect to the applied voltage for crosslinked HfO₂. Gr, graphene; SP, surface potential. Scale bar, 200 μm (e).

into van der Waals heterostructures. First, the semiconducting 2D MoS₂ dispersion was spin-coated onto a 300-nm-thick SiO₂/Si substrate so that we could evaluate its electronic properties. The resulting transfer characteristic of the as-synthesized MoS₂ thin film exhibited extreme electron-doped behaviour with an on/off current ratio $I_{\text{ON}}/I_{\text{OFF}} = 2 \times 10^2$ and a threshold voltage $V_{\text{TH}} = -21.6$ V, which was due to the considerable number of sulfur vacancies produced during the solution processing (grey curve in Fig. 2a)¹⁶. To minimize this undesired sulfur vacancy-induced electron doping, we performed a series of consecutive postprocesses, which included chemical treatment using bis(trifluoromethane) sulfonimide (TFSI) (red curve in Fig. 2a) and subsequent thermal treatment (blue curve in Fig. 2a). We also examined the electrical properties of the MoS₂ thin film containing the crosslinker that enables the PROMPT strategy. The resulting devices displayed indistinguishable electrical properties in comparison to the device without the crosslinker (green curve in Fig. 2a). Furthermore, an X-ray photoelectron spectroscopy (XPS) analysis of the MoS₂ thin film (Fig. 2b) revealed the consistent positions of the Mo⁴⁺ 3d_{5/2} and Mo⁴⁺

3d_{3/2} doublet peaks at 228.93 and 232.08 eV, respectively, and a Mo:S equivalent ratio of 1.95, regardless of the presence of crosslinkers⁴². A Kelvin probe force microscopy analysis was performed to measure the work function of the MoS₂ thin films before and after crosslinking. The average surface potential values extracted from the mapping image (top panel of Fig. 2c) were nearly identical: 4.73 eV for crosslinked MoS₂ and 4.72 eV for pristine MoS₂. These values are consistent with previously reported values^{43,44} (bottom panel of Fig. 2c). Further characterizations, namely AFM images and photoluminescence spectroscopy, revealed no notable changes in morphology or physical properties after crosslinking (Supplementary Figs. 10 and 11). All these results consistently demonstrate the negligible influence of the crosslinker on the electronic and optoelectronic properties of the MoS₂ thin film, which was due to the small crosslinker loading (5 wt%) in the film.

Similarly, the electrical properties of the graphene thin film were systematically investigated so that we could optimize the processing conditions for electrode formation. First, the thickness of the graphene thin film was controlled by the number of spin-coating iterations.

Iterating once, twice or three times resulted in average thicknesses of 38, 55 and 134 nm, respectively, as shown in Supplementary Fig. 12. The as-prepared graphene thin films were then annealed at 200 °C or 300 °C to remove solvent residues and improve the sheet-to-sheet contact. Figure 2d shows the resulting current–voltage characteristics of the graphene thin films with respect to their thickness and annealing temperature. The electrical conductance of the graphene sample annealed at 300 °C was about two orders of magnitude higher than that of the device annealed at 200 °C for all thicknesses. Specifically, the graphene thin film annealed at 300 °C had conductance values of 7.6, 10.2 and 14.3 μS after the first, second and third spin-coating iterations, respectively. Next, we investigated the influence of crosslinking on the graphene thin film. Notably, the average sheet resistance of the crosslinked graphene thin film was nearly identical to that of the pristine film. For example, the sample that was coated three times had an average sheet resistance of 8.6 k Ω per square before crosslinking, which marginally changed to 9.1 k Ω per square after the crosslinking (Fig. 2e). Figure 2f shows the Raman spectra of the graphene thin films processed under different conditions, namely the as-prepared film, the film annealed at 300 °C and the crosslinked film annealed at 300 °C. The as-prepared film exhibits distinct D and G peaks at 1,335 and 1,575 cm^{-1} , respectively, with a D to G intensity ratio of 2.3, suggesting that the high number of defects mainly formed during solution processing⁴⁵. As previously reported, thermal annealing effectively removes the oxygen functional groups and facilitates the realignment of the crystal structure. Consequently, the annealed graphene film had a reduced D to G intensity ratio of 0.77, and the crosslinked film also followed this trend by exhibiting a D/G intensity ratio of 0.85. Based on the optimization, this graphene thin film could be successfully used as electrodes for MoS₂ FETs (Supplementary Fig. 13). The implementation of graphene electrodes considerably improved the electrical characteristics of MoS₂-based FETs, yielding a high $I_{\text{ON}}/I_{\text{OFF}} = 1 \times 10^8$, a positive V_{TH} shift of 0.25 V and $\mu_e = 4.75 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These enhancements can be attributed to the reduced Schottky barrier height between the channel and electrode, which was mainly due to the smaller difference in the work function between graphene and MoS₂ in comparison to that between Au and MoS₂.

Finally, HfS₂ thin films were processed as a template for high- k dielectric HfO₂ through a post-thermal oxidation process. To optimize the dielectric properties, oxidized HfS₂, together with the impact of the crosslinking process, was thoroughly analysed using comprehensive characterization techniques, namely AFM, XPS, Raman spectroscopy and electrical property analysis. The thickness of the individual HfS₂ nanosheet decreased from 3.3 to 1.2 nm after oxidation (Supplementary Fig. 14) owing to a collapse of the atomic structures. Similarly, the average thickness of the HfS₂ thin films assembled under various conditions, namely different numbers of coating iterations, crosslinking and oxidation processes (Supplementary Fig. 15), decreased by 80% (ref. 7). Even after the crosslinking process, there were no major structural changes in either thickness or surface roughness compared with the pristine film, as shown in Supplementary Fig. 16. Additionally, the chemical compositions of HfS₂, HfO₂ and the crosslinked HfO₂ film were characterized using XPS analysis. Compared with HfS₂, for which S 2p doublets are evident and O 1s is negligible, the XPS spectrum of oxidized HfS₂ had two distinct O 1s peaks at 531.2 and 533.3 eV, which correspond to Hf–O and C–O bondings, respectively, whereas the S 2p doublets were diminished (Fig. 2g)⁷. Importantly, the XPS spectra of crosslinked HfO₂ revealed nearly identical peak positions and ratios for Hf 4f, S 2p and O 1s compared with the pristine HfO₂ film. The Raman spectra also confirm that the chemical properties of HfO₂ were maintained after the crosslinking process⁴⁶ (Supplementary Fig. 17). Subsequently, the dielectric properties of the crosslinked HfO₂ film, which had a thickness of 5.9 nm (obtained after ten coating iterations), were investigated by fabricating a metal–insulator–metal structure with Si⁺⁺/HfO₂/Au electrodes. Figure 2h shows the capacitance–frequency

curve, which exhibits a stable capacitance of 260.4 nF cm^{-2} within the frequency range 3 kHz to 1 GHz. The capacitance obtained is higher than that of other 2D dielectric thin films, such as hexagonal boron nitride ($\sim 245 \text{ nF cm}^{-2}$)⁴⁷. The crosslinked HfO₂ film exhibited a breakdown voltage of 4.5 V, which corresponds to a breakdown field strength of 7.6 MV cm^{-1} (Fig. 2i).

Electronic properties of FETs based on all 2D materials

The optimized photopatterning conditions for each semiconducting, metallic and insulating 2D thin-film preparation process enabled the fabrication of vertically stacked van der Waals heterostructures on a wafer scale. As shown in Fig. 3a, the unique role of the crosslinkers enabled all the MoS₂, graphene and HfO₂ thin films to be successfully photopatterned as semiconducting, electrode and dielectric layers, respectively, without affecting the preexisting patterns. Thus, this approach can create FET arrays on a 2-inch wafer. The detailed fabrication procedures are described in Methods. Figure 3b,c shows the electrical characteristics of the all-photopatterned FETs, namely the output and transfer characteristics. The output characteristics (drain current (I_D) versus drain voltage (V_D)) of the transistor for various gate voltages (V_G) clearly exhibited linear behaviour in the low V_D region, ideal contact formation and saturation in the high V_D region, with the highest I_D value of up to 496.9 μA . Figure 3c displays the representative electrical transfer characteristics (I_D versus V_G) of the FET on a logarithmic scale (black) and a linear scale (blue) at a fixed $V_D = 1 \text{ V}$. The FET exhibited a typical n-type transistor operation, with $|I_D|$ increasing abruptly as $|V_G|$ was increased positively. Notably, the transfer characteristics exhibited negligible hysteresis with good device metrics, namely an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of over six orders of magnitude and $\mu_e = 29.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which was derived from $I_D = (W/L)(V_D \mu_e C_i)(V_G - V_{\text{TH}})$, where W is the channel width (1,400 μm), L is the channel length (50 μm), C_i is the effective capacitance of the gate dielectric (260.4 nF cm^{-2} from Fig. 2h) and V_{TH} is the threshold voltage¹⁶. The negligible hysteresis between the forward and reverse sweeps indicates that crosslinking the 2D materials was highly beneficial, not only for realizing orthogonal multilayer patterning but also for enhancing the charge transport at nanosheet junctions (Supplementary Fig. 18).

The improved electrical properties of the electrochemically exfoliated MoS₂ channels were quantitatively demonstrated by extracting interfacial charge trap density values from the transfer curves of the FETs fabricated using various techniques, including conventional photolithography with a photoresist and inkjet printing. Compared with the conventional photolithography methods, the PROMPT approach yielded transistors with a lower trap density (~ 30 times) and negligible hysteresis. These electrical properties can be explained by the surface morphology of the MoS₂ thin film after orthogonal patterning, which had negligible chemical residue compared with a thin film patterned using photolithography (Supplementary Fig. 19). Moreover, the orthogonally patterned thin film had a substantially lower surface roughness (r.m.s. roughness $\sim 2.3 \text{ nm}$) compared with the thin film after photolithography (r.m.s. roughness $\sim 9.9 \text{ nm}$), facilitating the creation of a clean interface during the integration of electronically distinct layers and thereby improving the charge transport.

Because of these characteristics, which minimize the factors for charge trapping (for example, surface residue and interfacial disorder), note that the FETs based on PROMPT exhibited a negligible hysteresis comparable to that of mechanically exfoliated MoS₂ devices and a hysteresis superior to that of MoS₂ devices grown by chemical vapour deposition (Supplementary Table 1)⁴⁸. Although the extracted trap density of the inkjet-printed FETs is compatible with that of the PROMPT-fabricated FETs, the inferior on-current level (more than three orders of magnitude lower) requires further improvement for high-performance electronic applications. To systematically investigate the uniformity and scalability of the direct photopatterning

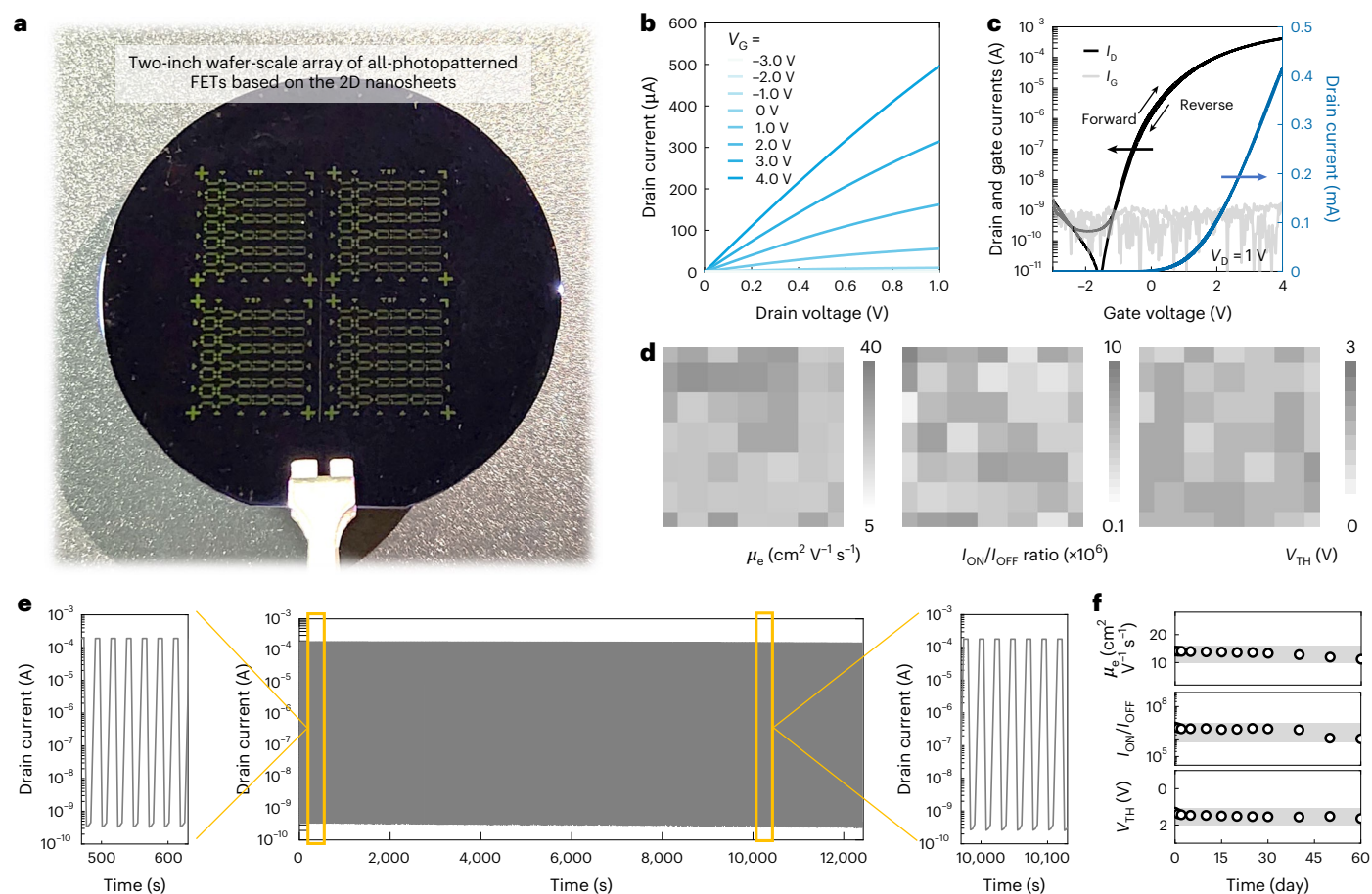


Fig. 3 | Electronic properties of FETs based on all 2D materials. **a**, Photographic image of a wafer-scale array of FETs based on all-photopatterned 2D materials and logic gates on a 2-inch Si wafer. **b**, Representative output characteristics of the FETs. **c**, Transfer characteristics of the optimized FET. **d**, 2D heat maps of the 49 FETs. Each device was randomly selected on the 2-inch Si wafer to

measure its carrier mobility distribution (left), on/off current ratio (middle) and threshold voltage (right). **e**, Operational stability of the 2D material-based FETs over 12,000 s of periodic inputs. **f**, Electron mobility, on/off current ratio and threshold voltage of the FETs fabricated with 2D van der Waals materials as functions of the exposure time in air under ambient conditions.

methods, the representative parameters for evaluating the electrical performance of a transistor, that is, μ_e , $I_{\text{ON}}/I_{\text{OFF}}$ ratio and V_{TH} , were extracted for 49 FETs fabricated on a 2-inch wafer, as shown in Fig. 3d. The transistor array exhibited a high uniformity with an average $\mu_e = 20.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, $I_{\text{ON}}/I_{\text{OFF}} = 1.36 \times 10^6$ and $V_{\text{TH}} = 1.6\text{ V}$ (the transfer characteristics of all 49 FETs are shown in Supplementary Fig. 20). A statistical 2D mapping image analysis of the representative parameters of the FETs revealed a small deviation in the electrical characteristics of the nearly equivalent devices, which may be largely attributed to the high spatial uniformity of the 2D nanosheets prepared by solution-based exfoliation and thin-film assembly¹⁶. The reported electrical performance of large-area 2D devices is compared in Supplementary Fig. 21 and detailed in Supplementary Table 2. We highlight that the electrical characteristics of devices based on the PROMPT approach are comparable to those of polycrystalline MoS_2 films grown by chemical vapour deposition, even at lower processing temperatures, and superior to those of previously reported solution-processed network devices fabricated on commonly used oxide layers.

Additionally, we investigated the operational stability of all-photopatterned FETs containing the crosslinker under repeated on and off states (bias stress testing). Square wave input pulses with $V_G = -1$ or 3 V and a constant $V_D = 1\text{ V}$ were applied to the device for more than 12,000 s, as shown in Fig. 3e. Notably, a negligible variation in the cyclic tests was observed during this evaluation of the long-term operational stability. Moreover, $I_{\text{ON}}/I_{\text{OFF}} > 10^6$ was maintained during the entire test. The environmental stability of the all-photopatterned

FETs was also investigated by monitoring the evolution of the transfer characteristics of the FETs under ambient conditions for 60 days. The resulting plot revealed negligibly compromised device characteristics (Supplementary Fig. 22). Figure 3f shows the representative device parameters plotted as functions of the ambient conditions. The resulting metrics, namely μ_e , $I_{\text{ON}}/I_{\text{OFF}}$ and V_{TH} , indicate that our photopatterned device exhibited notable environmental stability over 60 days. These operational and environmental testing results indicate that the proposed photopatterned FETs fabricated using 2D materials with a crosslinker attained excellent long-term stability without any additional encapsulation process. To further investigate the electrical stability of the FETs, bias stress testing was performed by monitoring the V_{TH} shift and I_D decay profiles with respect to time, as shown in Supplementary Fig. 23.

Applicability to various logic circuits

As illustrated in Fig. 3, the all-photopatterned FETs based on the solution-processed 2D materials exhibited high spatial uniformity and device performance, further enabling the demonstration of several logic gates, namely NOT, NAND and NOR gates. As illustrated in Fig. 4a, the NOT gate comprises two identical FETs connected in series. The voltage-transfer characteristics were evaluated by measuring the output voltage (V_{OUT}) as a function of the input voltage (V_{IN}) at a constant source voltage and various supply drain voltages (V_{DD}) of 0.4 – 2.0 V , as shown in the left panel of Fig. 4b. This logic structure clearly exhibited a typical signal inversion characteristic, which indicates tunable signal

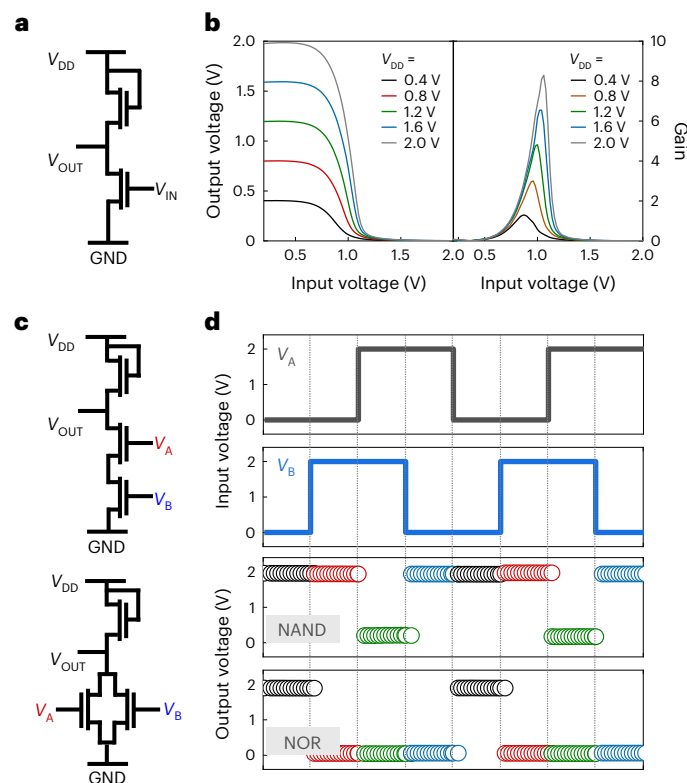


Fig. 4 | Applicability to various logic circuits. **a**, Electric circuit diagram of the NOT gate (inverter). **b**, Voltage-transfer curves (left) and corresponding signal inverter gain (right) of the NOT gate. **c**, Electric circuit diagrams of the NAND gate (top) and NOR gate (bottom). **d**, Input voltage combinations (upper two panels) and the corresponding output voltage signals of the NAND and NOR gates (lower two panels). GND, ground.

inversion, that is, V_{OUT} yielded the logic state 0 when V_{IN} was in the logic state 1 and vice versa. The extracted inverter gain value, defined as $|\partial V_{OUT}/\partial V_{IN}|$, from the corresponding NOT gate is plotted in the right panel of Fig. 4b. The peak inverter gain was ~ 8.3 with a sharp transition between the logic states 1 and 0 at $V_{DD} = 2.0$ V. This result demonstrates that the 2D material-based FETs fabricated by employing a photo crosslinker are suitable for logic operations because of the noticeable difference in the signal inversion.

Next, we designed and fabricated more complicated logic circuits, such as NAND and NOR gates. The scalability and uniformity of the 2D material-based, all-photopatterned FETs readily made them suitable for fabricating complex and high-performance logic gates. Figure 4c shows schematic circuit diagrams of the NAND gate (top) and NOR gate (bottom). The NAND gate was created by connecting three identical FETs in series, whereas the NOR gate was fabricated by connecting one FET in series and two FETs in parallel. The logic operations for both the NAND and NOR gates were evaluated by measuring V_{OUT} with a square waveform of V_{IN} (V_A and V_B), which was set to 0 V (logic state 0) or 2 V (logic state 1), as shown in the upper panels of Fig. 4d. The two voltage inputs (V_A and V_B) composed the four possible input V_{IN} combinations ((0,0), (0,1), (1,1) and (1,0)) at a constant $V_{DD} = 2.0$ V to induce a logic operation for the NAND and NOR gates. As shown in the lower panels of Fig. 4d, the NAND and NOR gates exhibited different V_{OUT} characteristics induced by the V_{IN} combinations. The NAND gate exhibited the logic state 0 only for the input logic combination (1,1) and the logic state 1 for the other three V_{IN} combinations ((0,0), (0,1) and (1,0)). Conversely, the NOR gate exhibited V_{OUT} in the logic state 1 only for the input logic combination (0,0) but exhibited V_{OUT} in the logic state 0 for the other three V_{IN} combinations ((1,0), (0,1) and (1,1)). Both the NAND and NOR

gates displayed reliable logic functions for all possible V_{IN} logic combinations over several repetitions. These experimental results indicate that FETs based on direct photopatterned 2D nanosheets can be used for complicated circuit designs and demonstrations.

Conclusions

We have shown that photo-sensitive crosslinkers can be used to pattern exfoliated 2D thin-film networks without affecting the prepatterned underlying thin-film networks. Photo-sensitive crosslinkers provide additional covalent bonding between van der Waals interfaced nanosheets, which improves charge transport through the nanosheet-to-nanosheet interfaces. We used this approach, which we refer to as PROMPT, to fabricate wafer-scale, all-photopatterned FET arrays based on solution-processed semiconducting MoS_2 , insulating HfO_2 (oxidized from HfS_2) and conducting graphene as a channel layer, dielectric layer and electrodes, respectively. The FETs based on solution-processed 2D MoS_2 thin-film networks exhibited an average field-effect mobility of $20.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and long-term device stability for over 60 days under ambient conditions without encapsulation. Finally, the wafer-scale FET arrays showed high spatial uniformity and were used to create various logic gates, namely NOT, NAND and NOR gates. Our approach offers a promising route for fabricating large-scale, high-performance electronic devices based on van der Waals heterostructure integration.

Methods

Electrochemical exfoliation of the 2D nanosheets

Bulk crystals of MoS_2 (HQ Graphene) and HfS_2 were electrochemically exfoliated using molecular intercalation to prepare the MoS_2 and HfS_2 dispersions. Intercalation was performed using an electrochemical cell with a two-electrode configuration. A bulk crystal and a graphite rod were employed as the cathode and anode, respectively. An electrolyte was formulated by dissolving tetraheptylammonium bromide (99.0%, Sigma-Aldrich) in acetonitrile (anhydrous, 99.8%, Sigma-Aldrich) at a concentration of 5 mg ml^{-1} . The applied voltage was set to 7 V, and the intercalation reaction proceeded for 1 h. After intercalation, the crystal was rinsed in ethanol and subsequently sonicated in a solution of PVP (molecular weight 40,000, Sigma-Aldrich) dissolved in dimethylformamide (99.5%, Daejung Chemical & Metals) at a concentration of 22 mg ml^{-1} for 30 min. Thereafter, the solution was centrifuged at $1,968g$ for 10 min to remove any unexfoliated crystals. Finally, the exfoliated nanosheets were washed with isopropyl alcohol (99.7%, Daejung Chemical & Metals) and then dispersed in chloroform (99.5%, Daejung Chemical & Metals). To prepare the graphene dispersion, an electrochemical cell was assembled with graphite foils (Alfa Aesar) to serve as the anode and cathode. The electrolyte was an aqueous solution of 0.005 M tetrabutylammonium hydrogen sulfate (97%, Sigma-Aldrich), and the pH was adjusted to 7 by adding a controlled amount of NaOH (98%, Sigma-Aldrich). A voltage of 10 V was applied for 20 min while the entire electrochemical cell was maintained in an ice bath to prevent overheating. After the reaction, the as-intercalated graphite was rinsed with ethanol and deionized water through vacuum filtration and then sonicated in a 22 mg ml^{-1} PVP/dimethylformamide solution for 30 min. The as-exfoliated solution was centrifuged at $1,968g$ for 10 min, rinsed with isopropyl alcohol three times and finally dispersed in chloroform.

Fabrication of the 2D material-based FETs

The heavily p-doped Si substrate was cleaned by sequential ultrasonication with acetone, isopropyl alcohol and deionized water for 20 min each. A mixture of HfS_2 nanosheets and 5 wt% crosslinker in chloroform was spin-coated ten times onto the as-prepared Si substrate inside an argon-filled glovebox at 2,500 rpm for 30 s. The resulting HfS_2 thin film was irradiated with UV light (254 nm, $1,000 \text{ W cm}^{-2}$) for 5 s through a photomask. After this photo-induced crosslinking, the HfS_2 area that was not exposed to UV light was removed by sonicating the sample in

fresh chloroform and then annealing it at 500 °C for 5 h under ambient conditions to convert it into insulating HfO₂. Subsequently, the as-prepared MoS₂ dispersion solution was mixed with the crosslinker in chloroform (95:5 wt% ratio) and spin-coated onto the patterned HfO₂ films at 2,500 rpm for 60 s inside a glovebox. The same process was used to expose the MoS₂ film to UV light (254 nm, 1,000 W cm⁻²) through a photomask, and the uncrosslinked MoS₂ areas were rinsed by sonicating the film in fresh chloroform and subsequently annealing it at 80 °C for 2 min to remove the residual solvent. The patterned MoS₂ films were functionalized by being dipped into a TFSI solution (95%, Sigma-Aldrich) in 1,2-dichloroethane (anhydrous, 99.7%, Sigma-Aldrich; 10 mg ml⁻¹) for 30 min and then thermally annealed at 250 °C for 30 min. Both the chemical TFSI doping and thermal annealing procedures were performed inside an argon-filled glovebox. Finally, a blended solution of graphene and the crosslinker (95:5 wt% ratio) was spin-coated onto the HfO₂/MoS₂ multilayers and photopatterned using the same crosslinking process. The resulting devices were then annealed on a hot plate at 300 °C for 30 min inside an argon-filled glovebox. This annealing process was required to impart metallic conductivity to the graphene patterns.

Characterization

The morphology of the 2D nanosheets was characterized by using optical microscopy (ECLIPSE LV100ND POL/DS, Nikon) and AFM (NX10, Park Systems) under ambient conditions. The photochemical reaction of the crosslinker in the 2D thin films was confirmed by Fourier-transform infrared spectroscopy (Bruker IFS-66/S, TENSOR27). The decomposition characteristics with respect to the temperature of the PVP and crosslinker were investigated using thermogravimetric analysis (Q50, TA Instruments). The surface potentials of MoS₂ and crosslinked MoS₂ were measured using a Kelvin probe force microscope (NX10, Park Systems) under ambient conditions. The Raman and photoluminescence spectra of both the crosslinked and uncrosslinked 2D thin films were collected using an Alpha300R spectrometer (WITec) under ambient conditions. The chemical composition and bonding states of the 2D thin films were analysed using XPS (ESCALAB 250 XI, Thermo Fisher Scientific). The electrical conductivities of the graphene and crosslinked graphene films were measured using a four-point probe (Keithley 2182A, 2634B and 6221). The specific capacitances of HfO₂ and crosslinked HfO₂ were measured using an inductance–capacitance–resistance meter (Agilent E4980A, Keysight). The electrical characteristics of the FETs and logic gates were investigated using a Keithley 4200A-SCS unit at 25 °C in vacuo (under 10⁻⁴ Torr).

Data availability

The data that supports the findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

J.H.C. and J. Kang initiated and supervised all the research. I.C.K. and J. Kim conducted and designed most of the experimental work and data analysis. J.W.M., S.K., H.J. and S.Y.P. assisted with the data analysis. J.Y.P., O.S., V.M. and Z.S. synthesized the materials. M.S.K. assisted with paper writing. All authors contributed to the writing of the paper. All authors discussed the progress of the research and contributed to editing the paper.

Competing interests

The authors declare no competing interests.

Additional information

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